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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,466	02/20/2004	Yakov Roizin	TSL-135	7443

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,466	ROIZIN ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohtani et al (US 20030157758).

Ohtani teaches the following claimed limitations as cited below:

1. A method for making an embedded semiconductor memory device comprising:

forming one or more diffusion bit line regions in a semiconductor substrate (Fig.65 (3));

then thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions (Fig.65 (5) and (0010))and

then forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions (Fig.63 (9 and 20).

2. The method of Claim 1, wherein the intermediate dielectric layer comprises silicon nitride (ONO film 9- Fig.63).

3. The method of Claim 1, further comprising depositing a top dielectric layer over the intermediate dielectric layer using a chemical vapor deposition process (0060).

4. The method of Claim 3, wherein the top dielectric layer is formed by depositing high-temperature silicon oxide (0087-thermal oxide 20).

5. The method of Claim 3, wherein the top dielectric layer is a high dielectric material, having a dielectric constant equal to 4 or greater (oxide/nitride).

6. The method of Claim 3, wherein the top dielectric layer is deposited at a temperature of about 750 to 850 degrees C (0068- thermal oxidation is carried out at such a temperature range).

7. The method of Claim further comprising implanting CMOS well regions through the intermediate dielectric layer and the bottom oxide layer in a first region of the semiconductor substrate (0070-71).

8. The method of Claim further comprising: removing the intermediate dielectric layer and the bottom oxide layer in the first region of the semiconductor substrate (0110); and then depositing

a top dielectric layer over the nitride layer and the first region of the semiconductor substrate using a chemical vapor deposition process (0111).

9. The method of Claim further comprising fabricating one or more high-voltage transistors in the first region of the semiconductor substrate, wherein the high-voltage transistors use the top dielectric layer as a gate dielectric layer (Fig.63 (33- becomes the gate- 20 is the gate dielectric).

10. The method of Claim 8, further comprising forming a sacrificial oxide layer over the first region of the semiconductor substrate after removing the intermediate dielectric layer and the bottom oxide layer, but before depositing the top dielectric layer (0109)

11. The method of Claim 9, further comprising fabricating one or more low-voltage transistors in the first region of the semiconductor substrate, wherein each of the low voltage logic transistors have a gate dielectric layer thinner than the top dielectric layer (Fig.63 (20)).

12. The method of Claim 1, further comprising forming shallow trench isolation regions in the semiconductor substrate prior forming the one or more diffusion bit line regions in the semiconductor substrate (Fig.63 (10).

15. The method of Claim 1, further comprising:
forming a conductive layer over the top dielectric layer(Fig.63 (33);

patterning the conductive layer to define a plurality of word lines that extend over the bit line oxide regions and the bottom oxide layer(0098); and

removing the top dielectric layer and intermediate dielectric layer located between the plurality of word lines (Fig.51 (11)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al (2003/0157758).

In reference to claims 13 and 14, Ohtani teaches the method of Claim ; however fails to teach wherein each of the bit line oxide regions has a thickness that is about 1.5 to 3 times larger than a thickness of the bottom oxide layer (claim 13) and further fails to teach wherein each bit line oxide region has a thickness in the range of about 50 to Angstroms (claim 14).

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they

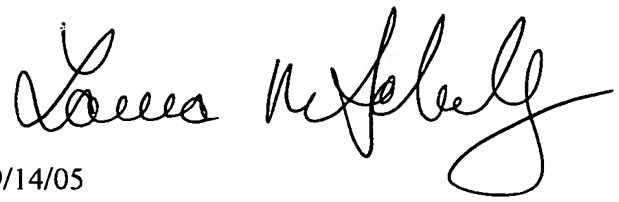
produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Laura M Schillinger
Primary Examiner
Art Unit 2813

09/14/05